Remarks

The instant Office Action dated July 29, 2008, notes the following rejections: claims 1, 3-8, 10-11 and 13 stand rejected under 35 U.S.C. § 112(2); claims 1, 3-5, 7-8, 10-11 and 13 stand rejected under 35 U.S.C. § 103(a) over Chang (US Patent No. 5,991,204) in view of Sharma (US Patent 5,488,579); and claim 6 stands rejected under 35 U.S.C. § 103(a) over Chang and Sharma and further in view of Chen (US Patent No. 6,091,104)

Applicant traverses the rejections and submits that the proposed combination of references fails to provide teaching or suggestion of all claim limitations, and further fails to either recognize or address the problems as addressed in the claimed invention. For example, none of the cited '204, '579 and '104 references has identified any issue relating to deposited dielectrics that are susceptible to undesirable growth (*i.e.*, the "bird beak" effect as discussed in Applicant's disclosure), or anisotropic etches that introduce undesirable control gate-channel characteristics.

In addition to the above, the '579 reference is directed to an inverted gate structure that is wholly unrelated to structure of the '204 reference and issues relating to the manufacture of the same. That is, the cited spacers in the '579 reference cannot and do not mitigate oxygen diffusion as claimed because they are not positioned to do so. Gate oxides 35 and 38 are completely exposed during any subsequent oxide growth, relative to the spacers 37, due to the inverted structure. In this regard, the '579 reference cannot teach spacers as claimed.

In view of the above, the cited combination of references does not teach or suggest all limitations in the independent claims. Further regarding the rejection of claim 4, Applicant submits that the rejection's assertion that the disclosed stripping requires "only removing the tunnel dielectric layer without removing (any of) the substrate" is unsupported by any citation and further does not appear to be disclosed in the '204 reference. In this regard, it appears that the Examiner has suggested that the '204 reference "inherently" discloses such limitations, but has done so in violation of the M.P.E.P. and relevant law, which requires evidence in support of such allegedly inherent teachings, and further that the missing limitations must "necessarily" be present. In this instance, and as is consistent with years of semiconductor manufacturing, many stripping processes do not operate as alleged to be inherent. Furthermore, as consistent with the

above discussion, none of the cited references appear to recognize problems relating to etching of the substrate. The rejection of claim 4 is thus also improper for these reasons.

Considering the above discussion, Applicant believes that the Section 103 rejections are improper and should be removed.

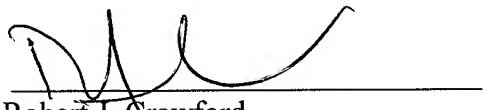
Applicant further believes that the rejections are no longer applicable to the claimed invention in view of the above amendments. That is, Applicant has amended the claims in a manner that is believed to be consistent with the claims as previously presented, and with the discussion in the specification (*see*, *e.g.*, figures 8-10 and paragraphs 0048-0053 for supporting embodiments). The cited references, alone or in combination, fail to disclose, teach or suggest various claim limitations. For instance, none of the cited references recognize issues relating to the mitigation of oxygen diffusion to a deposited inter-gate dielectric layer, or issues relating to protecting silicon underlying an access gate dielectric during anisotripic etching. Accordingly, the cited references do not disclose limitations directed to (using claim 1 as an example) "forming an access gate oxide ... using the spacers to mitigate the diffusion of oxygen to the deposited inter-gate oxide layer" to address the aforementioned and highly undesirable "bird beak" effect. The cited references further do not disclose "using the tunnel dielectric to protect portions of the substrate laterally adjacent to the floating gate" and "wet etching the tunnel dielectric to remove a portion of the tunnel dielectric laterally adjacent to the floating gate and expose a portion of the substrate where the tunnel dielectric has been wet etched," where such wet etching desirably preserves the underlying silicon surface (*see*, *e.g.*, new claim 14). Support for these limitations and related claims may be found in the above-cited portions of the specification.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 
Robert J. Crawford
Reg. No.: 32,122
(NXPS.442PA)